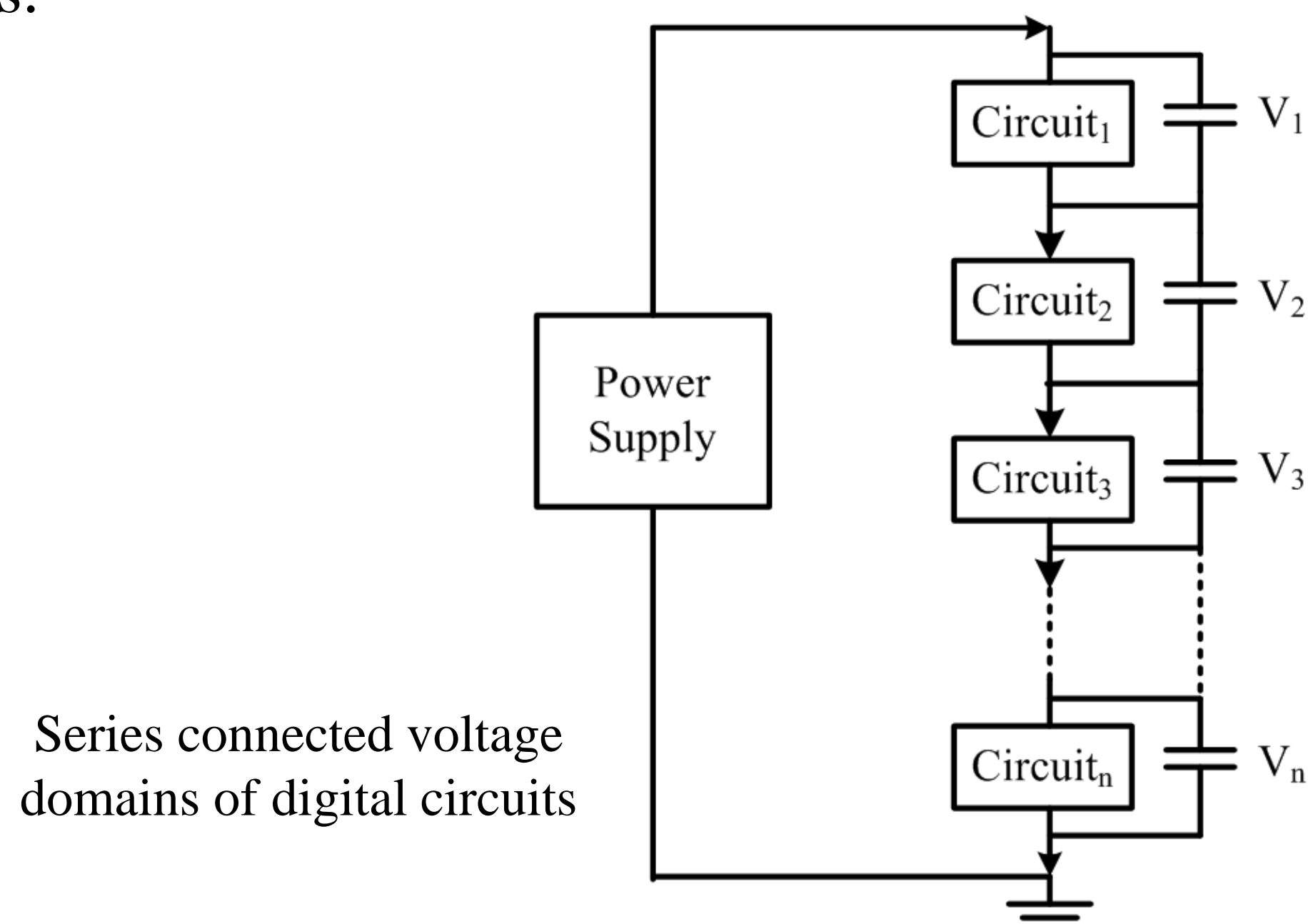


Overcoming the Power Wall: Connecting Voltage Domains in Series

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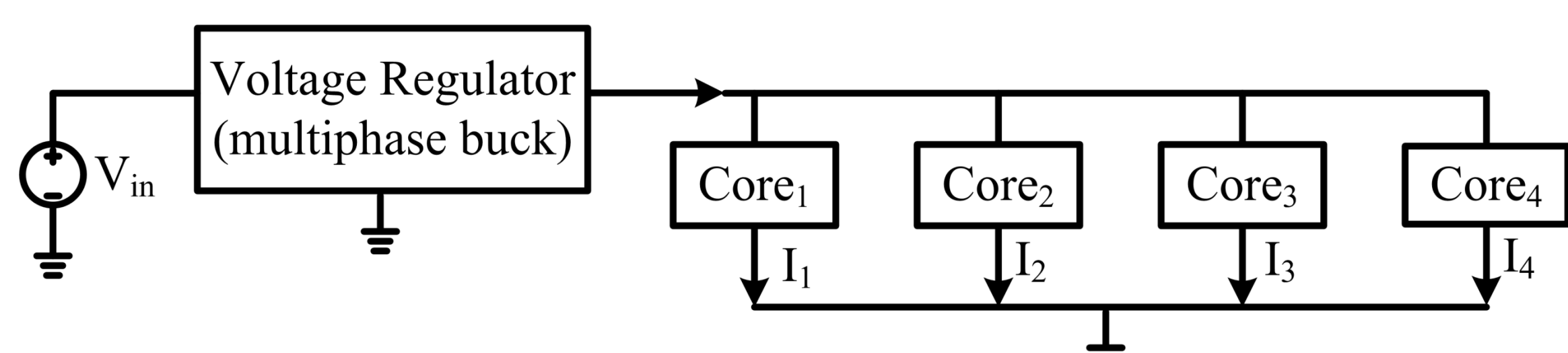
Objective

This poster presents a vision to reduce overall system energy consumption by connecting the voltage domains of digital circuits in series.

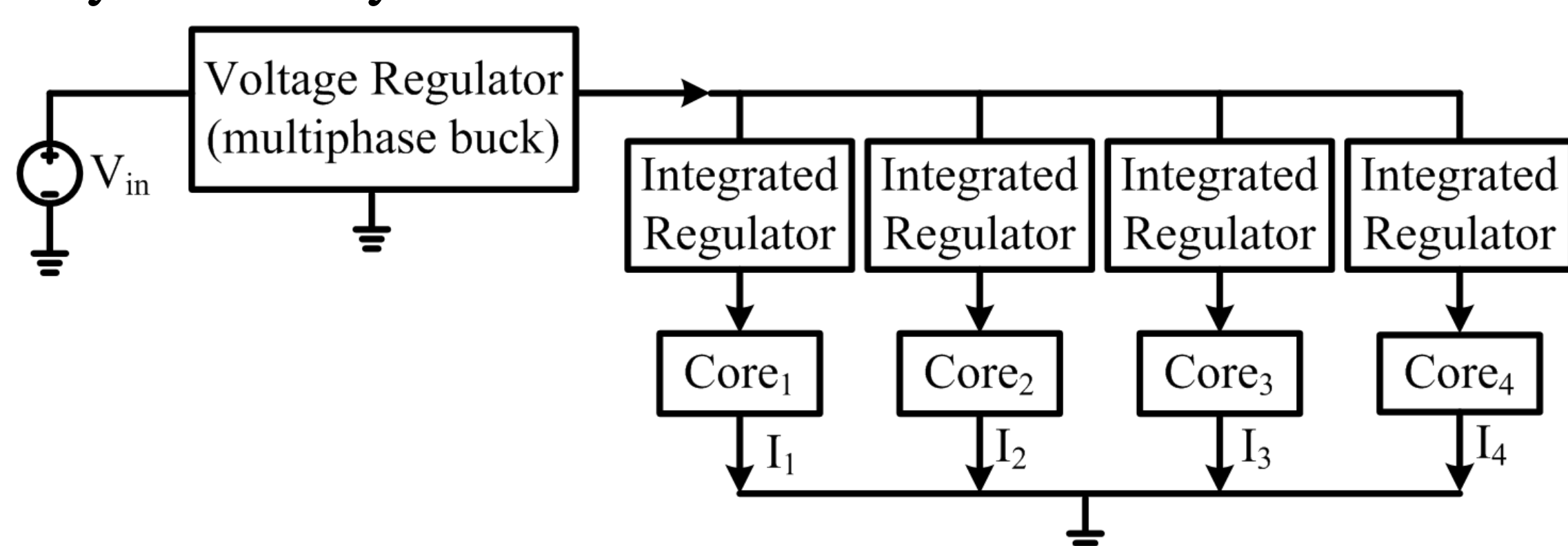


Background

- Reducing energy consumption and heat management overhead are key motivators for rethinking system-level design.
- Microprocessors trend towards computational parallelism (multi/many-core processors) and supply voltage reduction.



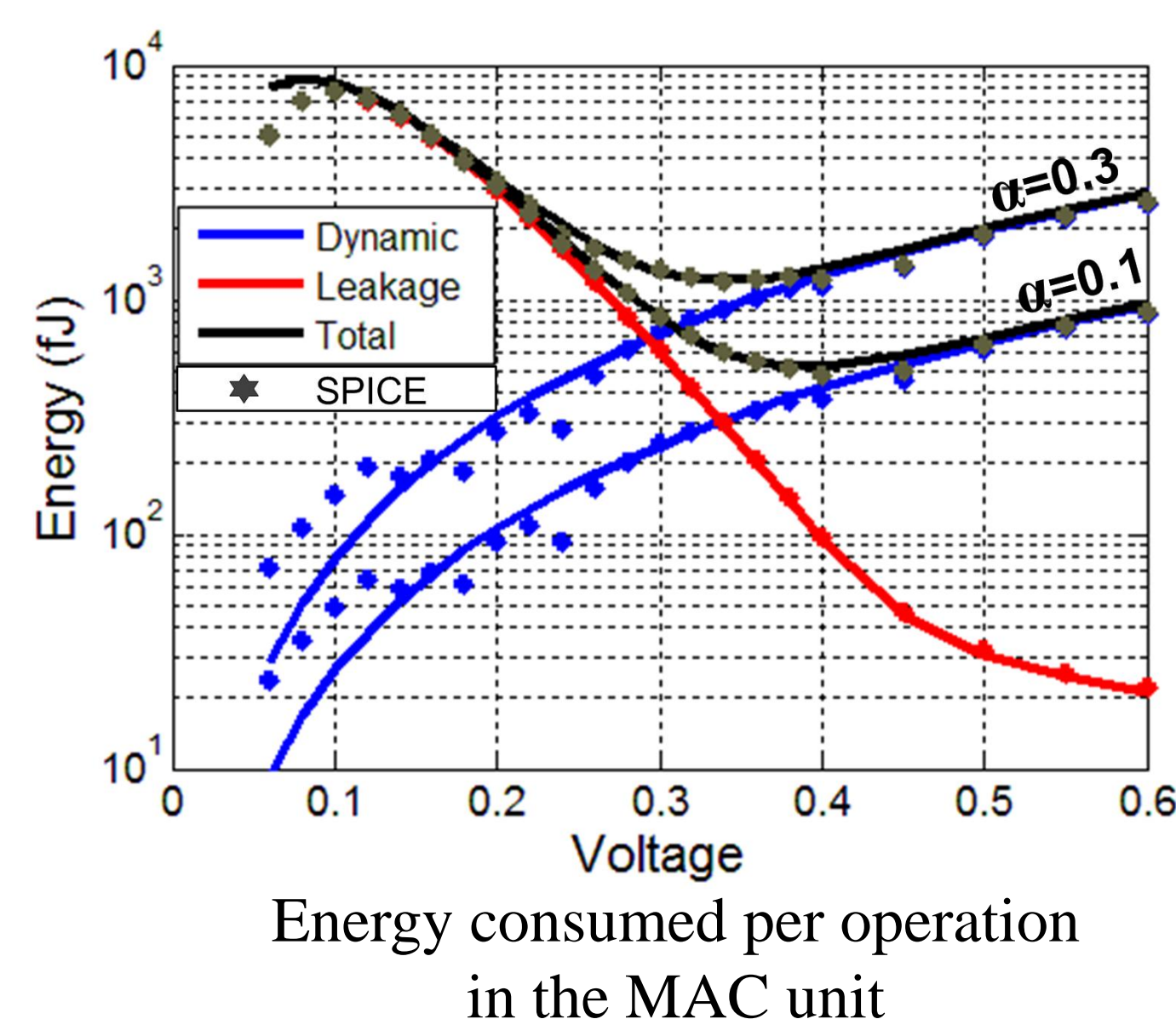
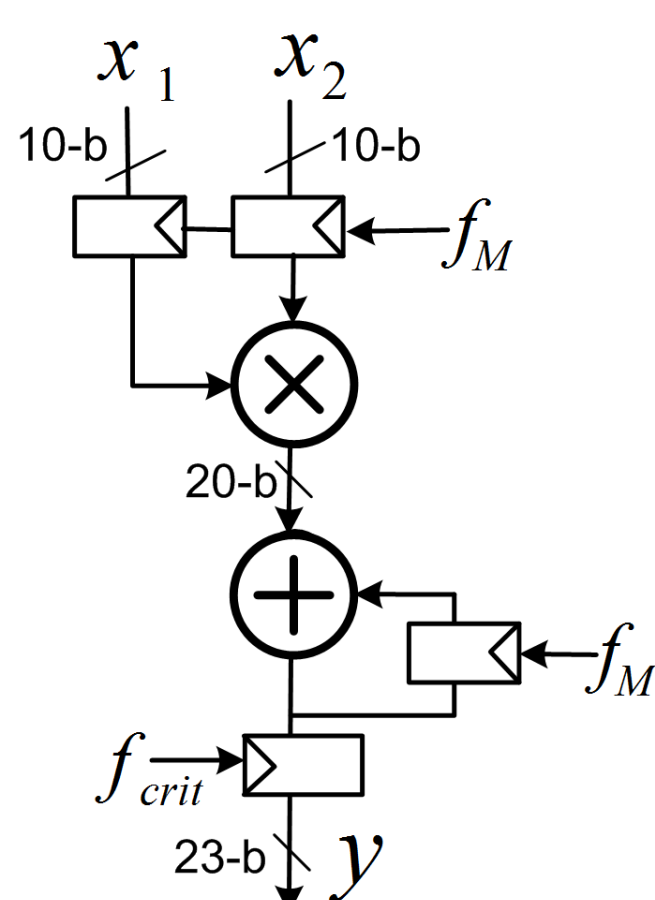
- Advanced designs with on-chip dc-dc converters enable independent voltage domains which may reduce energy consumption in digital circuit loads.
- However, the additional energy conversion stage reduces power delivery efficiency.



Core Energy Optimal Operating Point

- A minimum energy operating point exists in CMOS circuits (~0.3V).
- The energy consumed is the sum of dynamic and leakage energy.

$$E = E_{dyn} + E_{lkg} = \alpha CV_{dd}^2 + \frac{I_{OFF,V_{dd}} V_{dd}}{f}$$



Power Consumption Analysis

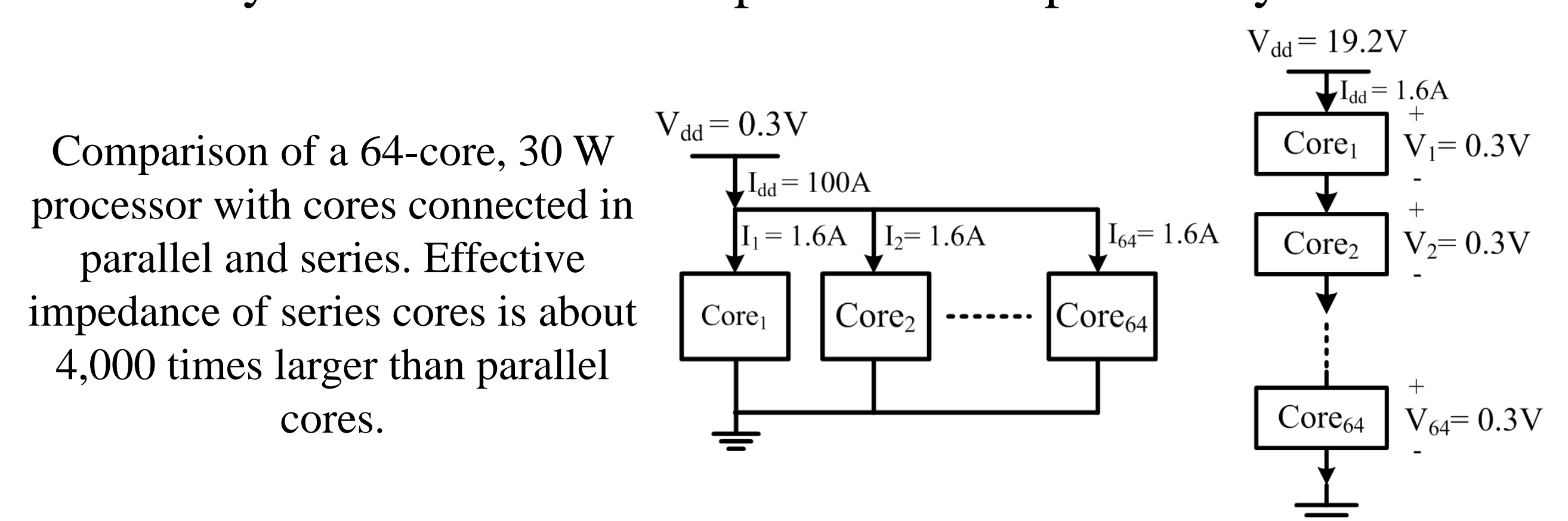
- Power consumption of systems (load and supply) with parallel connected and series connected voltage domains is compared.
- Independent voltage levels are enabled by the series connection.

$$P_{out,parallel} = \sum_{i=1}^N V_{dd,i} (I_{load,i}) = \sum_{i=1}^N \alpha_i C_{load,i} V_{dd,i}^2 f_{sw,i} \quad P_{out,series} = \sum_{i=1}^N I_{load,i} V_{dd,i} = \sum_{i=1}^N \alpha_i C_{load,i} V_{dd,i}^2 f_{sw,i}$$

- The power supply in a series system is more efficient (less current).

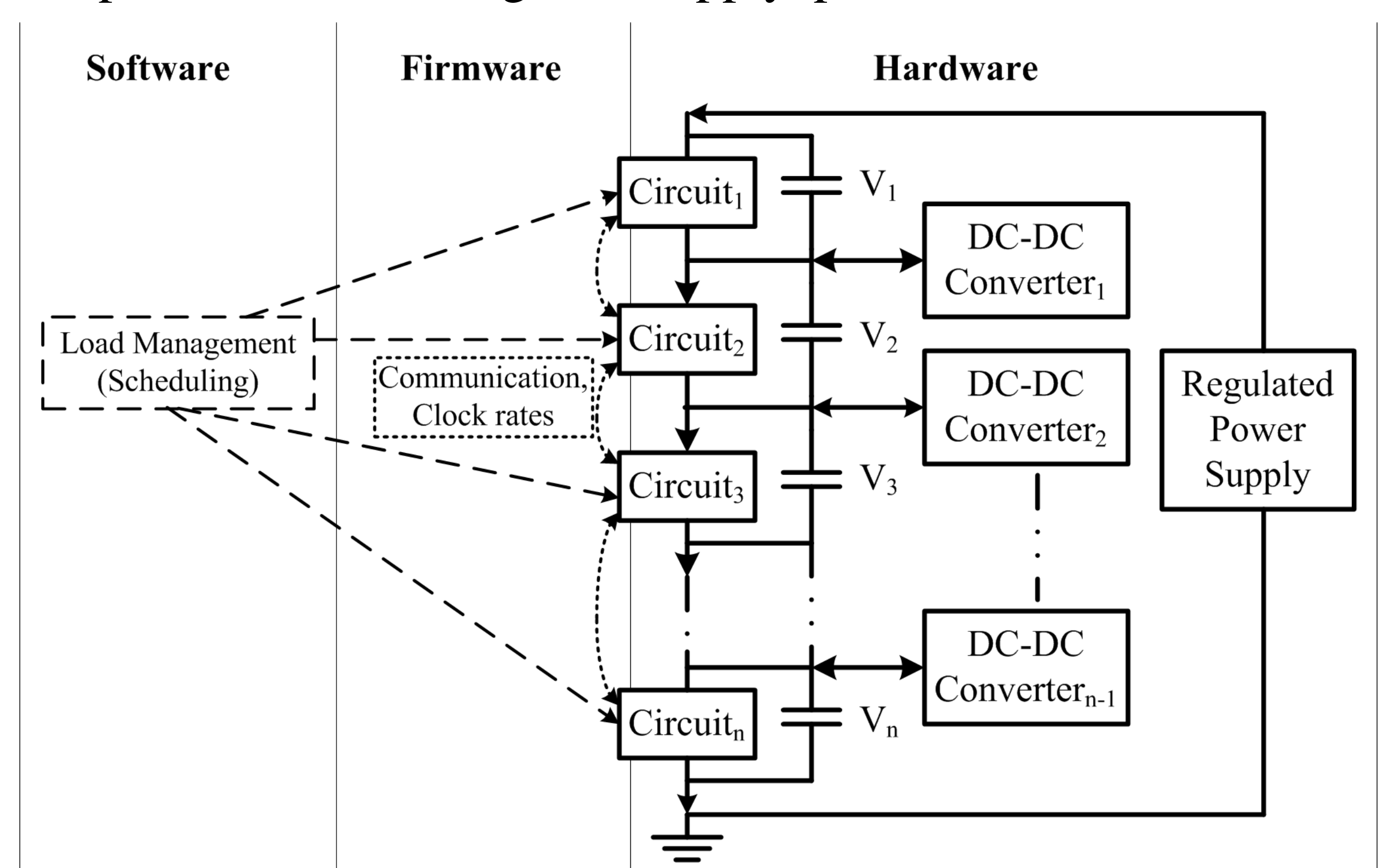
$$P_{cond} = (I_{load}^2 + \frac{\Delta I_{load}^2}{12})(r_L + Dr_1 + (1-D)r_2) \quad P_{sw} = \frac{1}{2} I_{load} V_{in} (t_{on} + t_{off}) f_{sw} + \frac{1}{2} C_{OSS} V_{in}^2 f_{sw}$$

- A series system consumes less power than a parallel system.



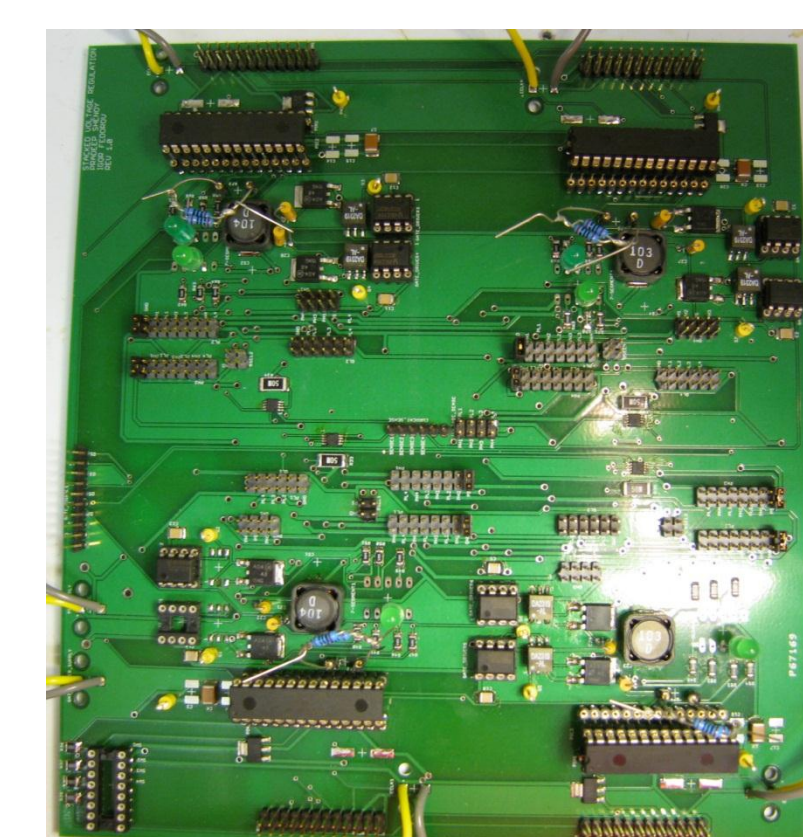
Regulation of Series Voltage Domains

- Balancing the computational load in software (scheduler)
- Adjusting clock rates, swapping tasks, and communication
- Local power electronics, global supply, protection



Conclusions

- Power delivery circuits and digital circuits can operate in their unique region of highest efficiency through series voltage domains.
- Voltage regulation is necessary and achievable using software, firmware, and hardware mechanisms that are efficient and reliable.
- Inter-core communication can be accomplished with capacitively-driven wires, optical interconnects, wireless communication, etc.



Experimental prototype with microcontrollers, data I/Os, and voltage regulation circuits

Selected References

- S. Rajapandian, X. Zheng, and K.L. Shepard, "Implicit DC-DC down conversion through charge-recycling," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 846-852, Apr. 2005.
- P. Jain, T.H. Kim, J. Keane, and C.H. Kim, "A multi-story power delivery technique for 3D integrated circuits," in *Proc. Int. Symp. Low Power Electron. Design*, 2008, pp. 57-62.
- A. Wang and A. Chandrakasan, "A 180-mV subthreshold FFT processor using a minimum energy design methodology," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 310-319, Jan. 2005.
- R. Ho *et al.*, "High-speed and low-energy capacitively-driven on-chip wires," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2007, pp.412-612.